

Zero-Noise Extrapolation via Cyclic Permutations of Quantum Circuit Layouts

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Increasing the utility of Noisy Intermediate-Scale Quantum (NISQ) devices requires efficient error mitigation, particularly for Variational Quantum Algorithms (VQAs) where accurate expectation values dictate gradient reliability. In this work we propose a novel Cyclic Layout Permutations based Zero Noise Extrapolation (CLP-ZNE) protocol for such a task. The method leverages the inherent non-uniformity of gate errors in NISQ hardware to extrapolate the expectation value, averaged over cyclic circuit layout permutations, to the level of zero noise. Crucially, we prove that this method cancels all linear-order noise contributions. The main steps of CLP-ZNE protocol are sketched in Figure 1.

In contrast to the foundational layout-permutation protocol introduced in [1] scaling as $O(n!)$ for n qubit circuit, CLP-ZNE requires execution of only $O(n)$ and at most $O(n^2)$ different circuit layouts for circuits of one-dimensional and arbitrary connectivity, respectively. When benchmarked against noise channels modeling the IBM Torino quantum computer, the method reduces a typical error in expectation values of $n = 12$ qubit circuits by an order of magnitude, outperforming standard unitary folding ZNE. Demonstrating robust mitigation of both depolarizing and T_1/T_2 relaxation processes, CLP-ZNE provides a highly scalable, hardware-aware pathway to improve VQA trainability on present-day NISQ hardware. The complete theoretical framework and numerical benchmarks are detailed in our manuscript [2].

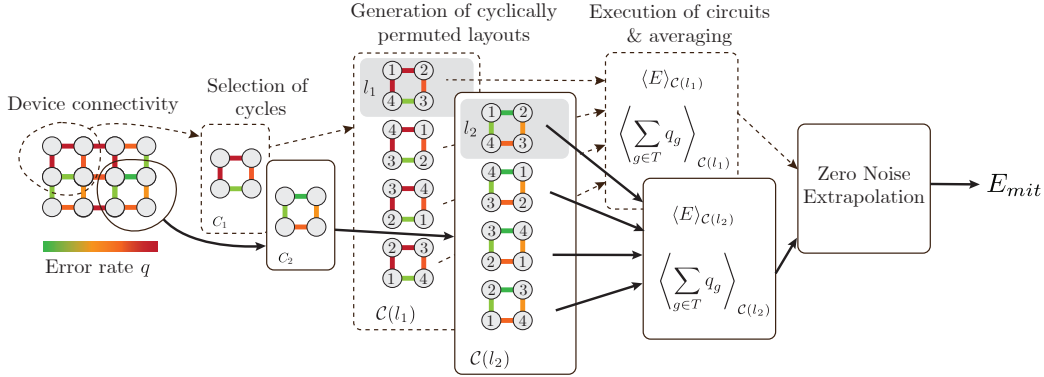


FIG. 1. **Schematic illustration of the proposed CLP-ZNE protocol applied to a four-qubit circuit.** Circles represent physical qubits, while edges denote available two-qubit couplings, color-coded by their individual error rates q . Numbers on qubits denote assignment of abstract qubits from the circuit into the qubits of the device.

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- [1] Alexey Uvarov, Daniil Rabinovich, Olga Lakhmanskaya, Kirill Lakhmanskiy, Jacob Biamonte, and Soumik Adhikary. Mitigating quantum gate errors for variational eigensolvers using hardware-inspired zero-noise extrapolation. *Phys. Rev. A*, 110:012404, Jul 2024.
 - [2] Zahar Sayapin, Daniil Rabinovich, Nikita Korolev, and Kirill Lakhmanskiy. Zero-noise extrapolation via cyclic permutations of quantum circuit layouts. *arXiv preprint arXiv:2511.02901*, 2025.

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